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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,493	04/15/2005	Ralf Brederlow	10808-234	9085

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BRINKS HOFER GILSON & LIONE
INFINEON
PO BOX 10395
CHICAGO, IL 60610

EXAMINER	
ABRAHAM, FETSUM	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/531,493	BREDERLOW ET AL.	
	Examiner	Art Unit	
	Fetsum Abraham	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The specification teaches the following in the Brief Summary Text:

[0022] In a next development, the field-effect transistor is a planar field-effect transistor, i.e. the area which is effective for the control of the gate electrode lies parallel to the insulating layer. In addition to HDD terminal regions (highly doped drain), the field-effect transistor also contains, if appropriate, LDD terminal regions (lightly doped drain) or auxiliary terminal regions and/or so-called pockets or halos, which are designated as auxiliary doping regions here.

Claim 3, however states that The circuit arrangement as claimed in claim 2, wherein at least one of: the field-effect transistor is a planar field-effect transistor, the transistor contains auxiliary terminal regions, which have a doping with the same conduction type as terminal regions of the transistor but with a dopant concentration that is smaller by at least one order of magnitude, the transistor contains auxiliary doping regions, which are arranged at least one of near the terminal regions or near the auxiliary terminal regions and which have a doping with a different conduction type at least one of than the terminal regions or than the auxiliary terminal regions or the control electrode adjoins a region containing a metal-semiconductor compound

As for claim 5, the dependency of the claim in relation to claims 2 and 4 is unclear. This examination assumes that the claim depends on both claims.

As for claim 6, the dependency of the claim in relation to claims 2 and 5 is unclear. This examination assumes that the claim depends on both claims.

Clearly, the underlines section of the text above separates said auxiliary terminal regions from auxiliary doping regions, while the specification seems to indicate both expressions as the same layer/s in the structure.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,9-15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murade (6569717) in view of Tsu et al (6,294,420).

As for claim 1, the document discloses the primary reference teaches the following:

An integrated circuit arrangement comprising: an electrically insulating layer (12), and at least one sequence of regions which forms a capacitor and which contains, in the order specified: a portion of an electrode region near the insulating layer (the lower electrode (1f)), the other portion being layer (80a)), a dielectric region (2), and an upper electrode region remote from the insulating layer (3b), the insulating layer arranged in a plane, the capacitor and at least one active component of the integrated circuit arrangement being arranged on the same side of the insulating layer, the electrode region (1f) near the insulating layer and an active region (1a') of the transistor component being arranged

in a plane which lies parallel to the plane in which the insulating layer (12) is arranged, and the capacitor and the active component forming a memory cell.

The prior art discloses all subject matter except said " insulation region" and said " processor"

So far as said insulation region is concerned, the element is not well defined in the specification as to which element in the structure exactly it was. No numerical identification seems to have been related to said region for one to fully understand its location in the overall structure. The examiner assumes layers (26,28) to be the insulation region claimed in the claimed invention, so far as the effort to understand the region sis concerned. To that understanding, the prior art also has such the claimed structure (so far as understood) in the extension of the composite insulation layer (2), (composed of gate insulation layer and capacitive dielectric layer) to the right surface of the lower capacitive electrode (1f) and the left side surface of the source region (1d) of the transistor. Clearly, the portion of the composite insulation layer in the perspective sidewalls defined above are of the same material to that of the insulating substrate (12), so called as insulating layer by applicant and is also attached to the insulating layer (12).

Therefore, it would have been obvious to one skilled in the art to conclude that the prior art indeed has insulation region (the sidewall insulations described above) as part of an insulation layer supporting the active and passive components because the region is of the same material type and in contact with the insulation layer.

As for the claimed processor, the following is what was taught in the specification:

Brief Summary Text:

[0033] In another development, the circuit arrangement contains at least one processor

containing a multiplicity of logical switching functions. If, in one configuration, the circuit arrangement additionally contains a multiplicity of DRAM memory units (Dynamic Random Access Memory) beside the processor, then a term that is also used is an embedded memory. In order to fabricate this circuit arrangement, in addition to the process steps and masks that are necessary anyway for fabricating the logic, only a small number of additional process steps and additional masks are required for fabricating the capacitor or the transistors that are electrically conductively connected thereto.

The primary art discloses all subject matter claimed but may have been silent on said processor. However, the secondary reference teaches the following:

Detailed Description Text (38):
A memory array of the present invention could also be embedded in a larger integrated circuit device. An embedded memory is a memory array and its associated control circuitry on the same integrated circuit as a substantial amount of logic. FIG. 4c has been included to illustrate a simple block diagram of an embedded memory. In this example, a DRAM array is included along with a processor (e.g., microprocessor, digital signal processor, specialty processor, microcontroller), another memory array (e.g., SRAM, non-volatile memory such as EPROM, EEPROM, flash memory, PROM, ROM, another DRAM array) and other logic circuitry. These particular blocks have been chosen to illustrate the wide variety of other logic, which could be included. Any combination of the devices could be included.

Therefore, it would have been obvious to one skilled in the art to reconfigure the prior art memory structure into one that can be characterized as embedded memory structure (defines as a memory structure formed in the same wafer as the controller circuits), since such structures integrate memory arrays with controller circuits in the same wafer, thereby greatly minimizing circuit density and material waste.

As for claim 2, the control gate (3a) of the transistor and the upper electrode remotely (3b) located from the insulating region are of the same material type and the gate insulation layer (2) and the composite capacitive dielectric layers surrounding electrode (3b) are of different thickness. Note that the composite capacitive dielectric layer has an upper portion above the capacitive electrode (3b) and a lower portion under the same.

As for claim 9, the insulating layer in the primary reference is silicon dioxide.

As for claim 10, like in all DRAM structures, the controller in the second reference is a microprocessor.

As for claim 11, the claimed method of forming represents the method by which the primary DRAM is formed. The semiconductor layer portion that makes the capacitive lower plate is a patterned semiconductor piece. No active transistor element or storage capacitor associated with memory cells is formed without patterning process on an insulating substrate. An insulating substrate may cover an entire wafer, but individual pixels in an array structure formed on the wafer must be patterned in order to separate from each other.

As for claim 12,the primary art involves at least applying one auxiliary layer (LDD layer) to the semiconductor layer prior to patterning because the patterning stages of capacitive electrodes take place after the formation of the LDDs, and a thermal oxidation in order to form a rounding oxide since a uniformly oxidized upper and side surfaces forms the composite insulation layer composed of the gate insulation layer, a portion of the capacitive dielectric layer and the sidewalls attached to the source region and the lower capacitive plate.

As for claim 13, LDD regions called as auxiliary terminal regions by applicant have lower doping density than the source and drain regions called by applicant as terminal regions.

As for claim 14, the doping process of said terminal regions (source/drain) regions of the transistor in the primary reference is performed at least after the formation of the electrode region remote from the insulating region or after the patterning of the control electrode, simply because lower layers must be formed before higher layer are formed in the structure. Although ion implantation can be performed to the source/drain regions through the gate insulation layer and in rare cases through the gate insulation and gate layers in situations where the gate electrode is used as a mask in the process, the primary reference seems to have the active layer, the drain in particular and the doped capacitive electrode (lower electrode) as being formed by the same doping process because the drain conductivity type and the lower electrode conductivity type are the same and both elements have exactly the same height. This safe assumption eliminated ion implantation process so far as at least the drain and the electrode are concerned because the remote capacitive electrode (32b) would not have allowed the ion implantation process through it to dope the layer under the capacitive dielectric layer and form a lower capacitive electrode.

As for claim 15, the uncovered semiconductor region where the central electrode is formed on through a contact layer (8a) in the primary reference is structurally metal-semiconductor type silicide at least at the interface level with the underlying drain region.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murade (6569717) in view of Tsu et al (6,294,420) and further in view of Sudo et al (5,555,520).

The first two references disclose all subject matter claimed but may have been short of exposing one of the capacitive plates as being a monocrystalline layer. However, Sodo et al show a DRAM structure ion the front page having a monocrystalline capacitive electrode (see the Title). Therefore, it would have been obvious to one skilled in the art to use such a layer as capacitive electrode in DRAM cells, since the practice provides a crystally uniform electrode short of crystal defect induced problems such as current leakages from capacitive electrodes to the neighboring elements in memory structures.

As for the claimed substrate carrier adjoining the insulating layer that supports the active and passive components and the other side of the insulating layer adjoining the capacitive electrode, the primary reference shows the claimed features fully.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Fig. 26 in PN: 6,525,556.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
2/17/06